

ABSTRACT

A semiconductor storage device according to the present invention comprises one or more memory planes 8 comprising a plurality of memory blocks 9, and a block selection circuit for decoding an block address signal for selecting the memory block 9 from the memory plane 8 to select the memory block, generates a dummy block address for selecting a dummy block that is different from the selected block address and a defective block address of a defective block by a predetermined logical operation targeted for a specific partial bit in address bits of the selected block address when the defective block is contained in the memory plane. A bit line connected to the selected memory cell selected by the selected block address and a bit line in the dummy block are connected to differential input terminals of a sense amplifier circuit 9.